PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Nishant Sinha

Serial No.: 10/668,914

Filed: September 23, 2003

For: PROCESS AND INTEGRATION SCHEME FOR FABRICATING CONDUCTIVE COMPONENTS, THROUGH-VIAS AND SEMICONDUCTOR COMPONENTS INCLUDING CONDUCTIVE THROUGH-WAFER VIAS

Confirmation No.: 2525

Examiner: W. Lindsay Jr.

Group Art Unit: 2812

Attorney Docket No.: 2269-5859US

VIA ELECTRONIC FILING
July 31, 2007

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On June 26, 2007, the Office mailed a communication in the above-referenced application in which an additional statement of reasons for allowance was presented. That statement follows: "examiner believes this references [sic] [U.S. Patent 4,605,471 to Mitchell] is only missing the steps of forming a partial via and the introduction of a filler."

It is respectfully submitted that use of the term "steps" in the above-stated reasons for allowance is inapplicable to the allowed claims, which are drawn to "intermediate semiconductor

device component[s]" rather than methods. Further, the scope of each allowed claim should be based upon its plain language, rather than the above-stated reasons for allowance, and the full scope of equivalents available to the recited elements.

Respectfully submitted,

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